

MS-7038

Version 1.0A
3/29/2004 Update

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.0G & Above

System Chipset:

Intel Springdale - GMCH (North Bridge)
Intel ICH5 (South Bridge)

On Board Chipset:

CLOCK -- Cypress CY28405

On Board Chipset:

BIOS -- FWH EEPROM 4M
AC'97 Codec -- REALTEK ALC655
LPC Super I/O -- W83627THF
LAN - REALTEK RTL8110S/8100C

Main Memory:

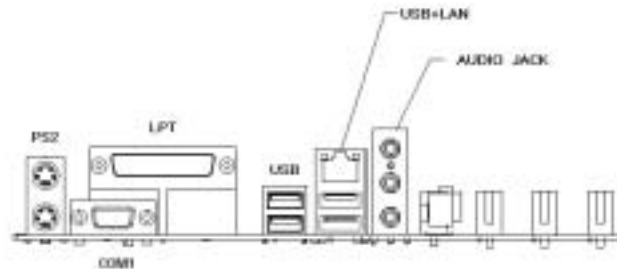
DDR * 2 (Max 4GB)

Expansion Slots:

PCI2.3 SLOT * 3
AGP4X/8X SLOT * 1

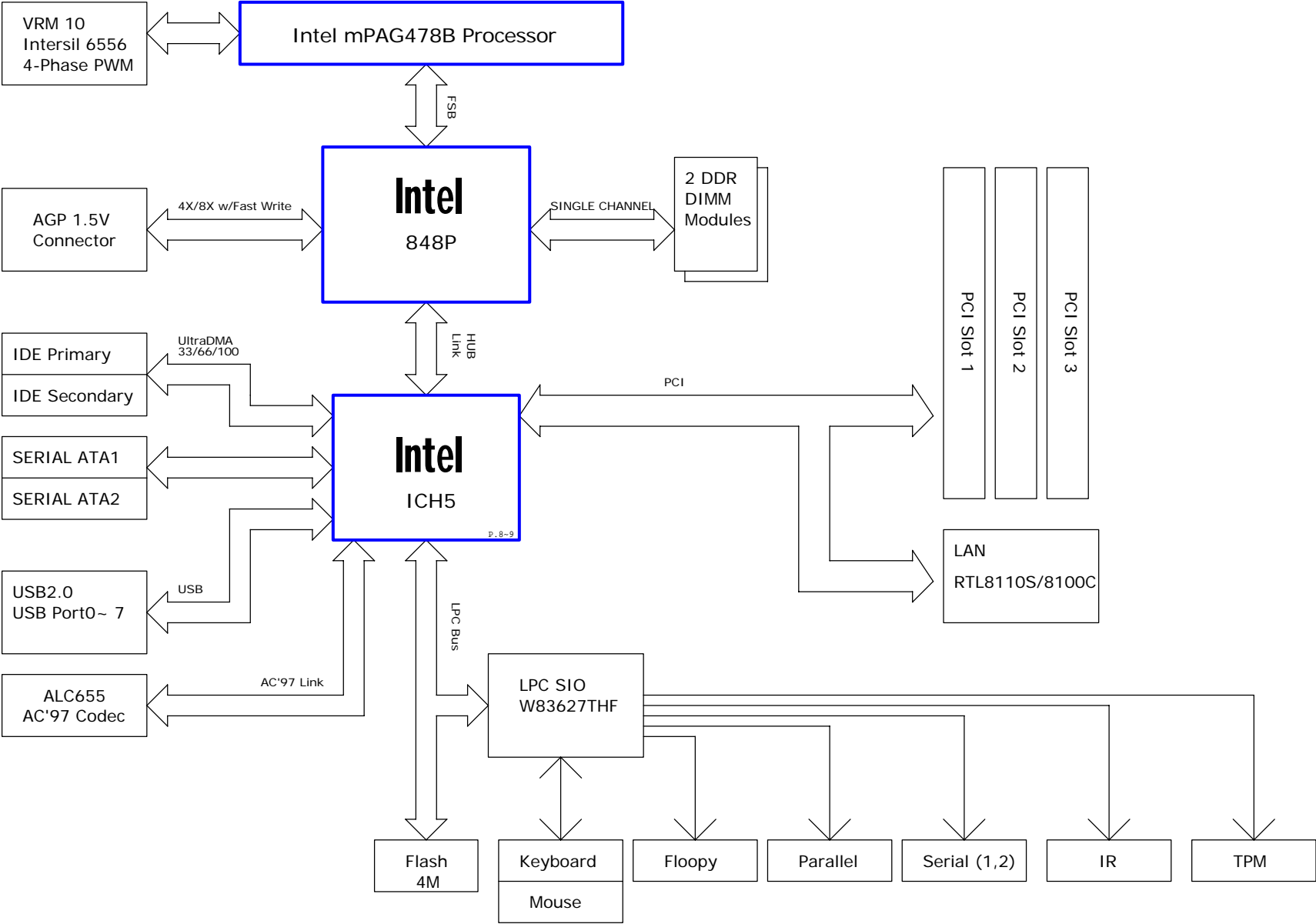
Intersil PWM:

Controller: HIP6556A
Driver: HIP6602B * 2
FMB 1.5 SPEC.



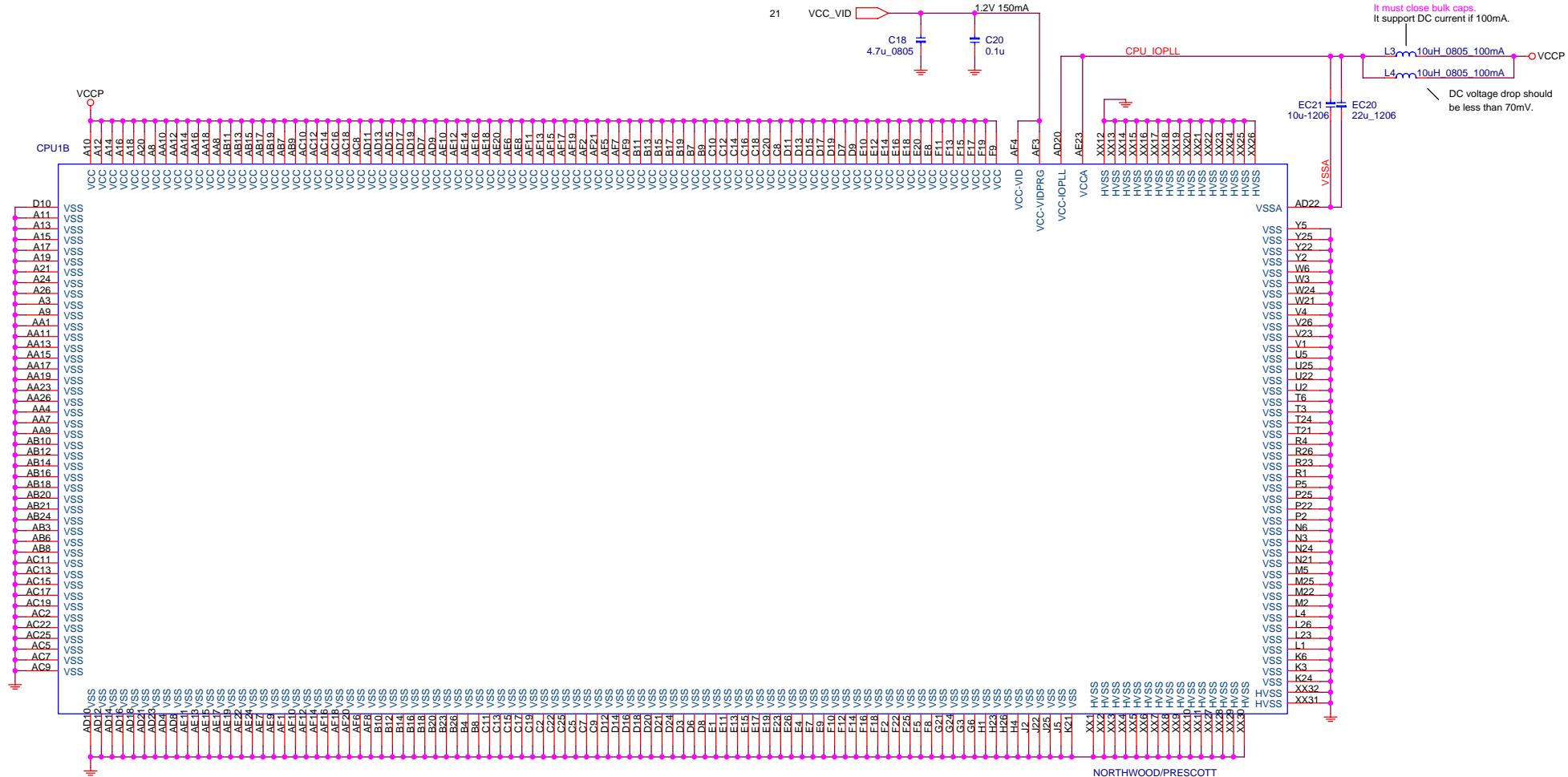
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Block Diagram

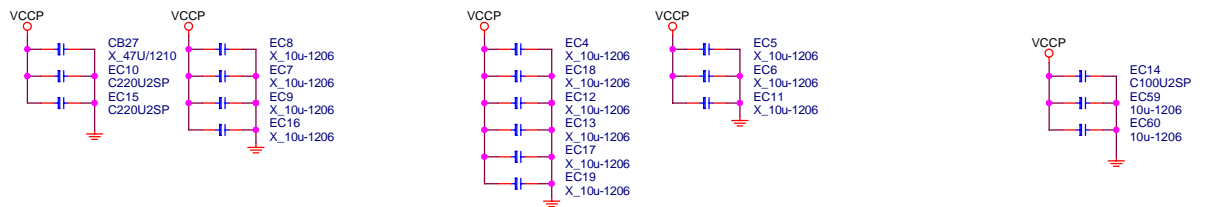


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Intel mPGA478B - Power



CPU DECOUPLING CAPACITORS

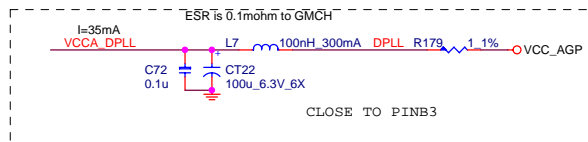
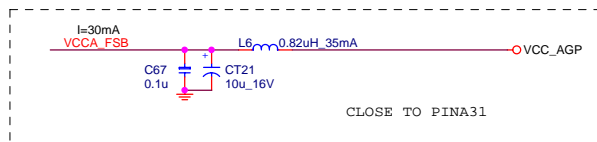
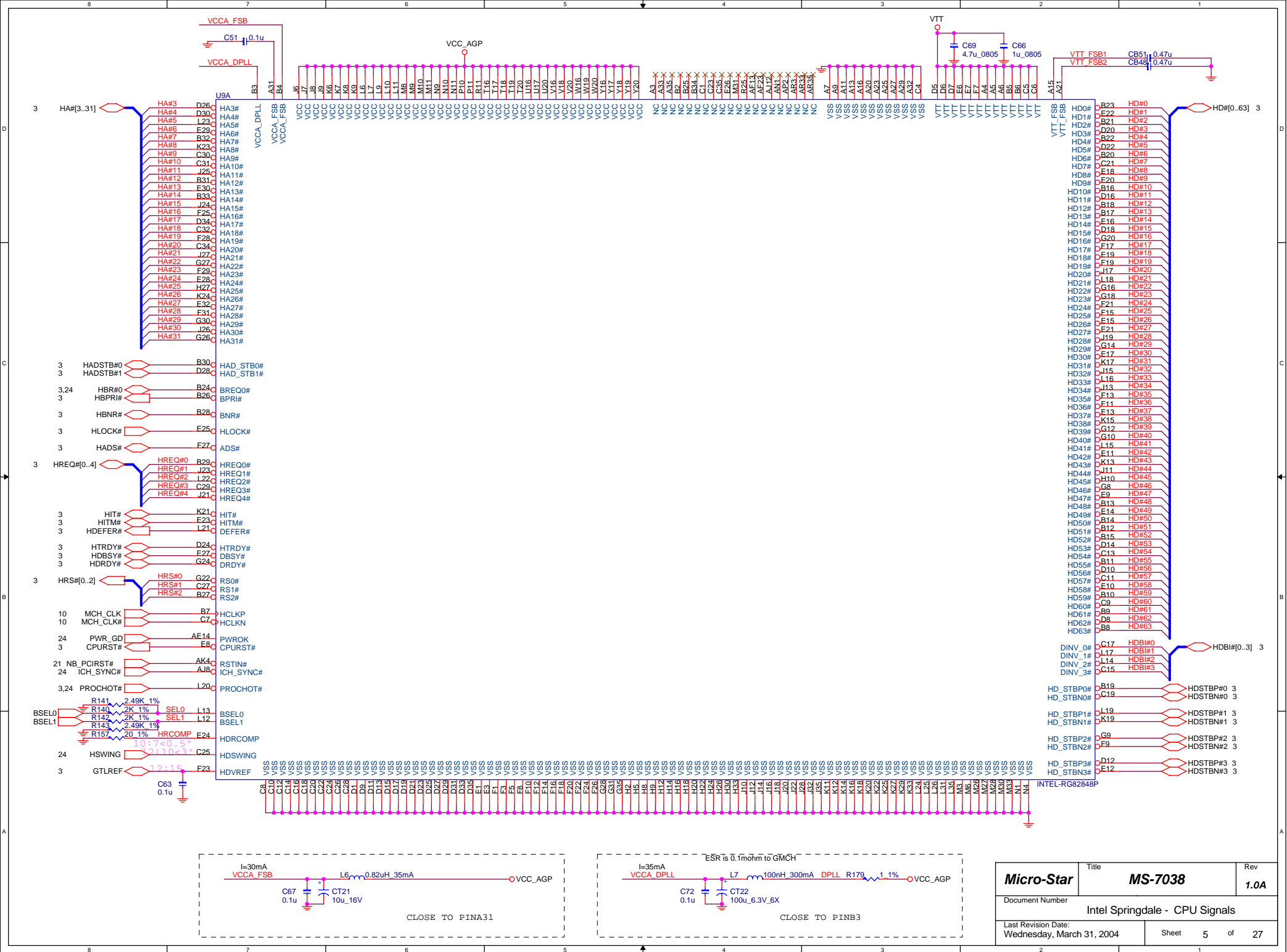


4pcs Place these caps within socket cavity

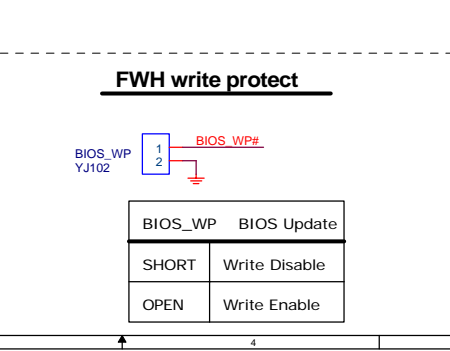
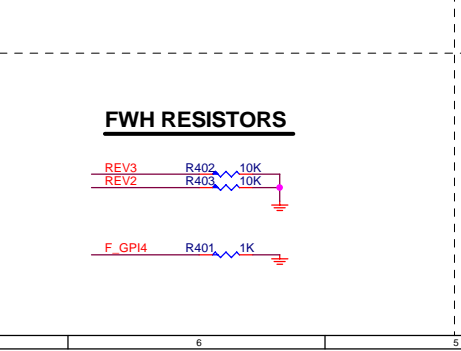
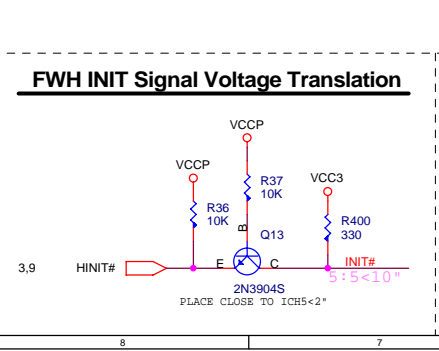
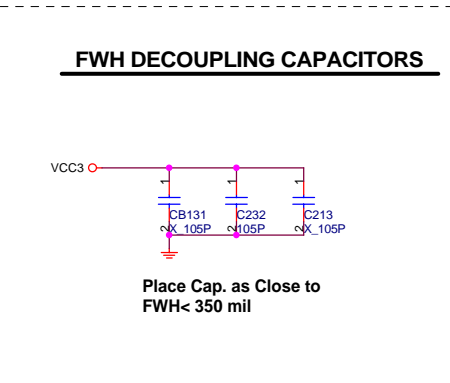
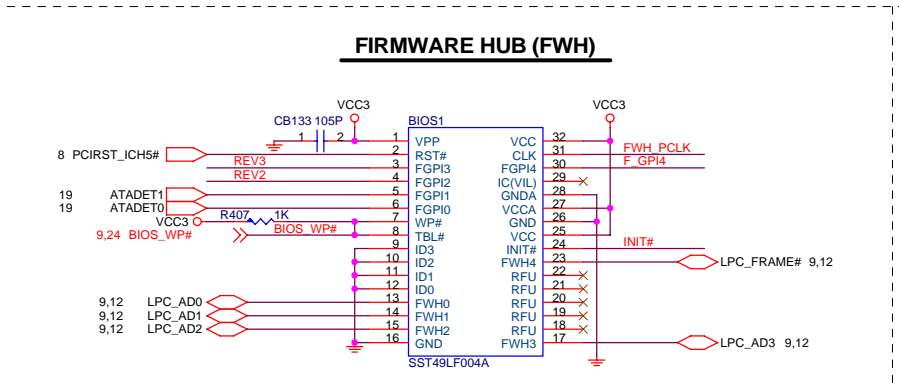
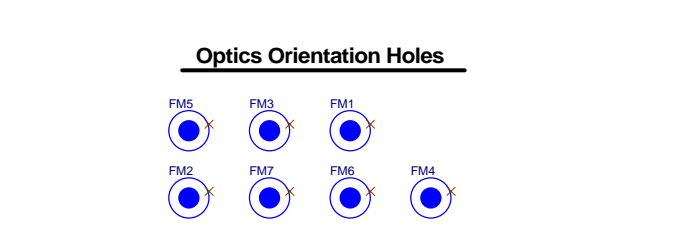
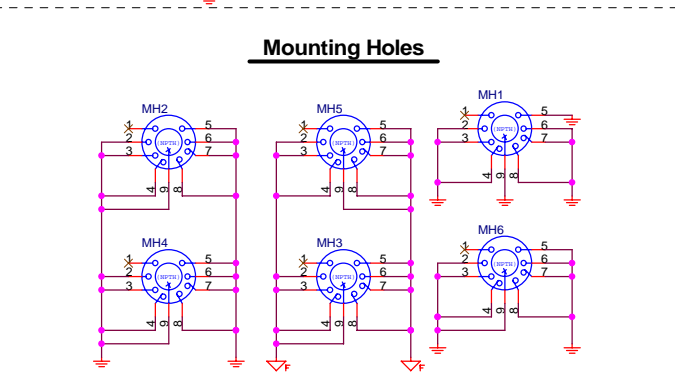
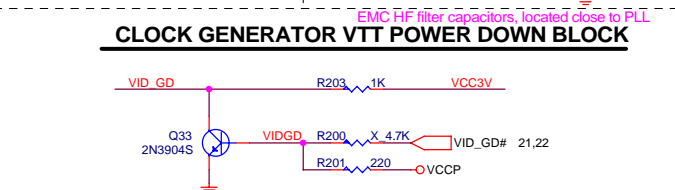
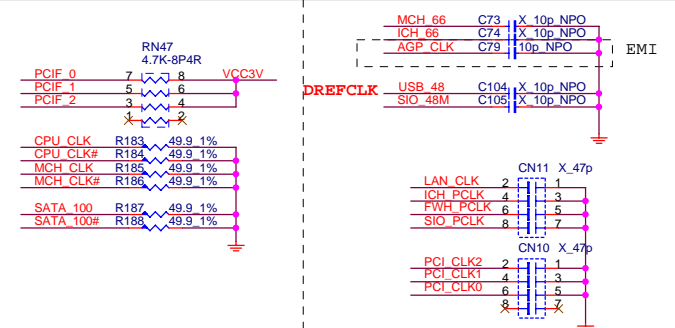
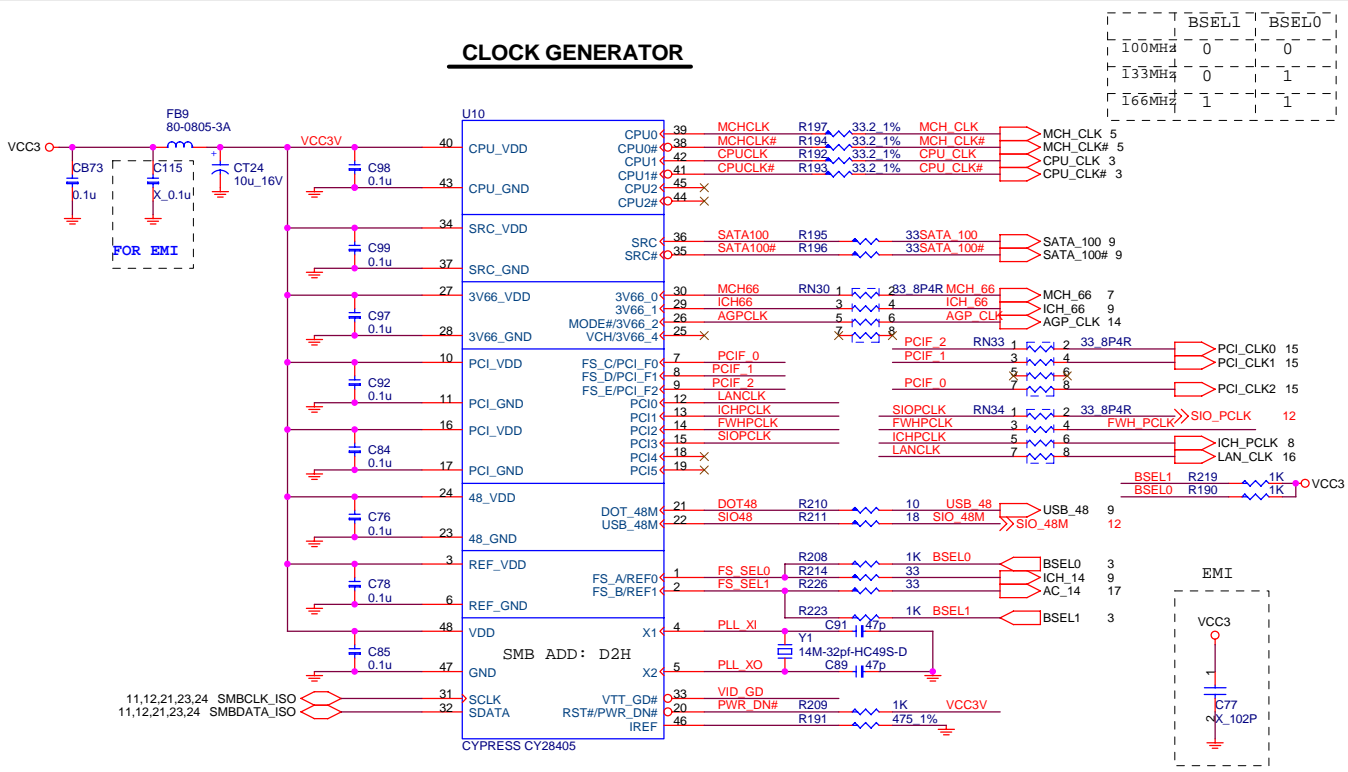
19pcs Place these caps within north side of processor

9pcs Place these caps within south side of processor

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Intel mPGA478B - Power		
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Micro-Star	Title	Rev
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Simulation

BIOS_WP	BIOS Update
SHORT	Write Disable
OPEN	Write Enable

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DDR DIMM1

SIGNALS

POWER

DECOUPLING CAPACITORS

ADDR.=1010000B(A0H)

DDR DIMM2

SIGNALS

POWER

ADDR.=1010001B(A2H)

DDR Termination Resistors

SIGNALS

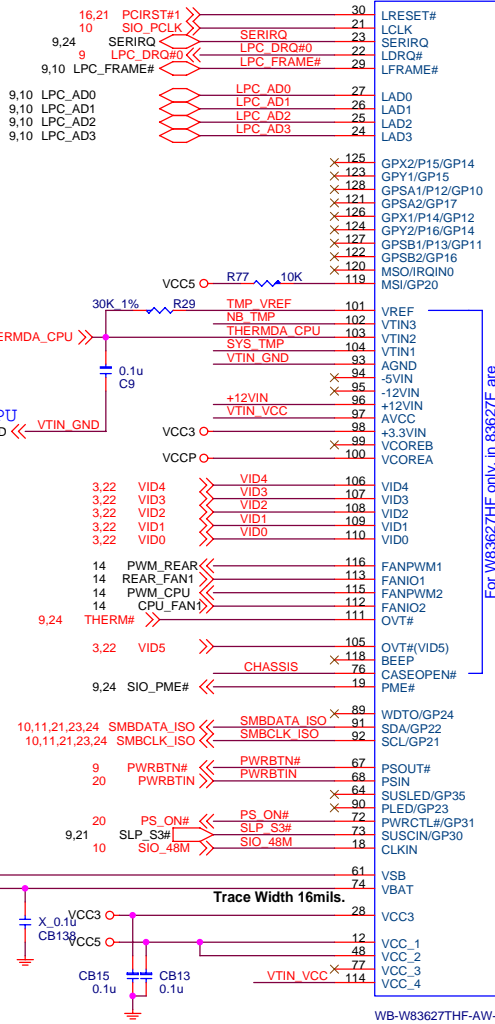
POWER

DECOUPLING CAPACITORS

Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

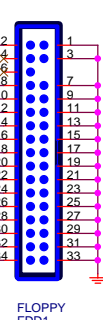
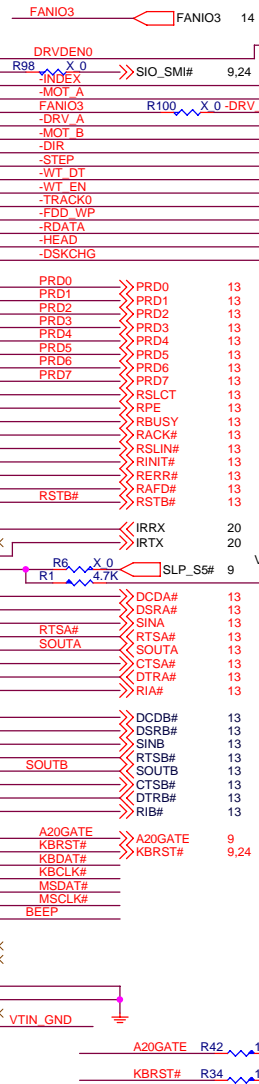
Micro-Star	Title	MS-7038	Rev	1.0A
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LPC SUPER I/O W83627HF/THF

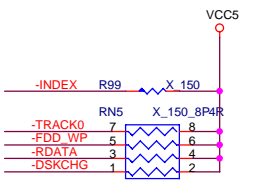


For W83627HF only, in 83627F are NC

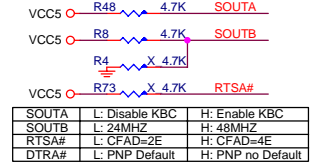
WB-W83627THF-AW-VG



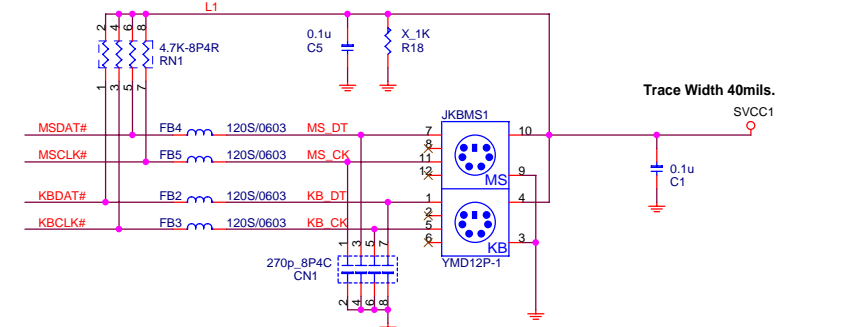
FLOPPY CONNECTOR



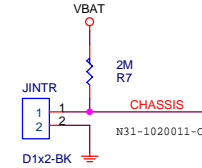
SUPER I/O STRAPPING RESISTOR



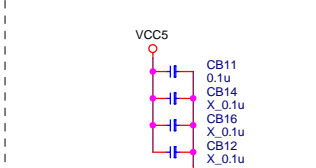
PS2 KEYBOARD & MOUSE CONNECTOR



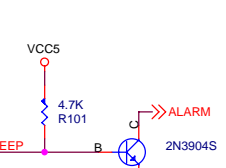
Chassis Intrusion



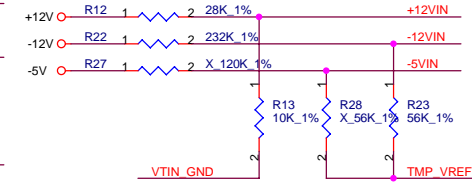
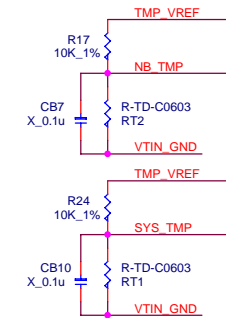
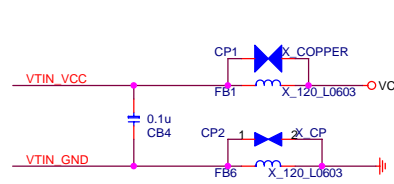
DECOUPLING CAPACITORS



SPEAKER BLOCK



THERMAL RESISTOR BLOCK



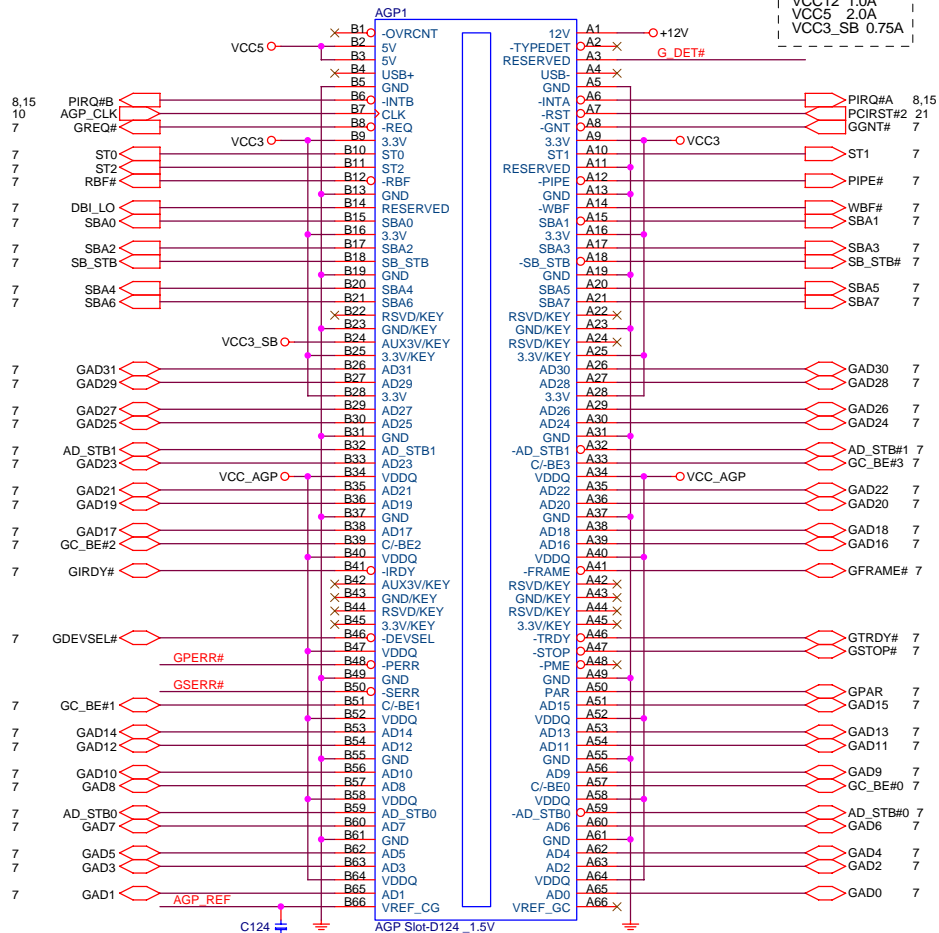
NOTE: LOCATE CLOSE STATUS PANEL

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AGP 1.5V 1X/2X/4X/8X SLOT(AGP VER:3.0)

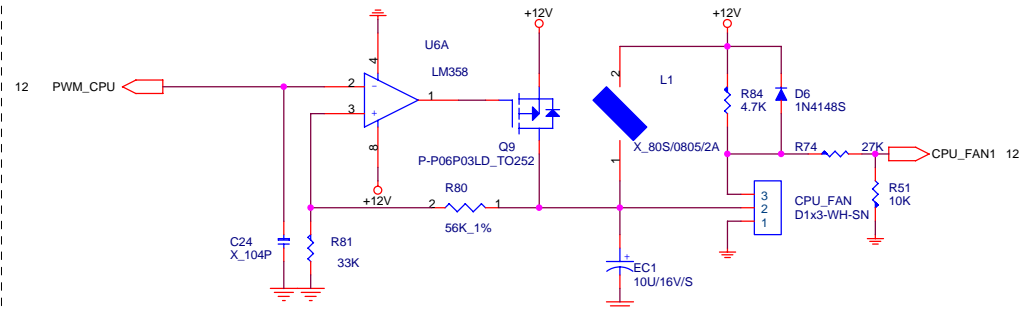
VCC5 = 60mils trace / 15 mils space

AGP Slot Imax
VCCg 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A
VCC3_SB 0.75A

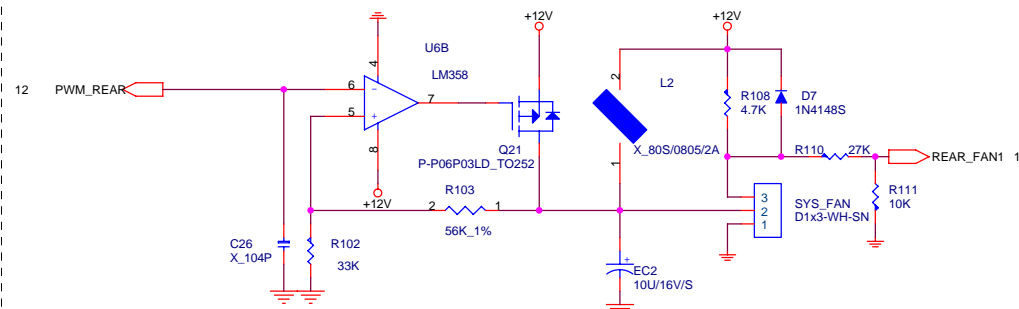


PIRQ#A / PIRQ#B

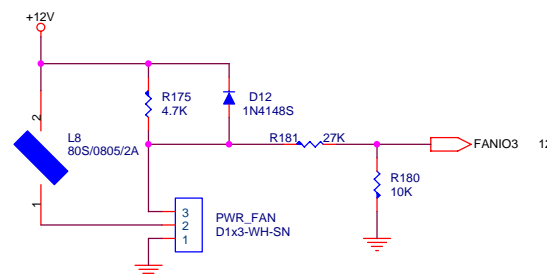
CPU FAN



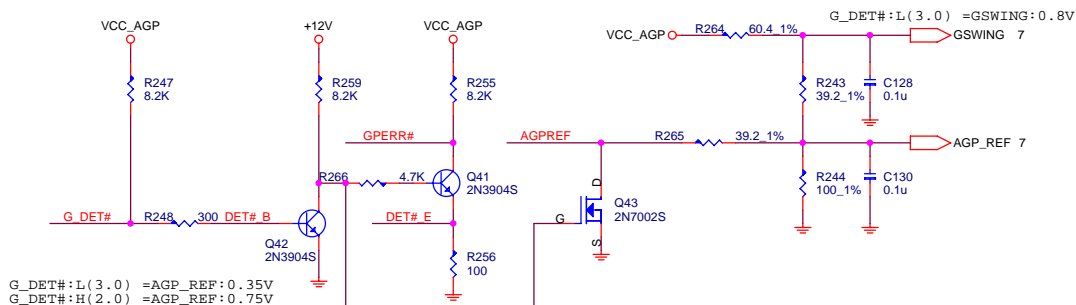
SYSTEM FAN



PWR FAN



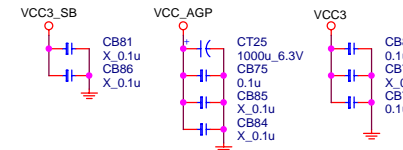
Springdale Reference & Swing Voltage Circuit



AGP TERMINATION RESISTORS

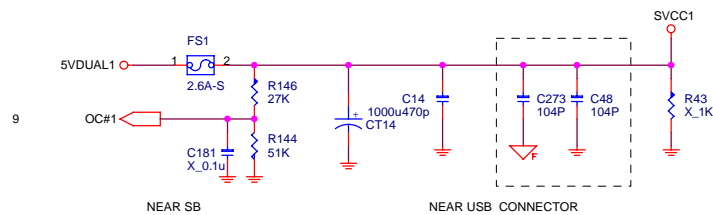
LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS

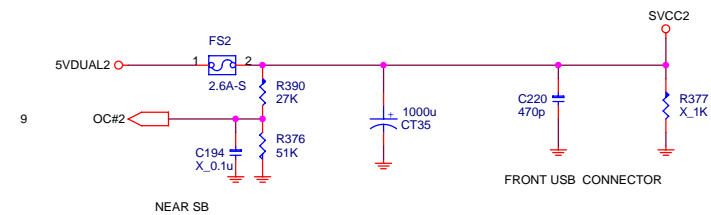


Micro-Star	Title	MS-7038	Rev	1.0A
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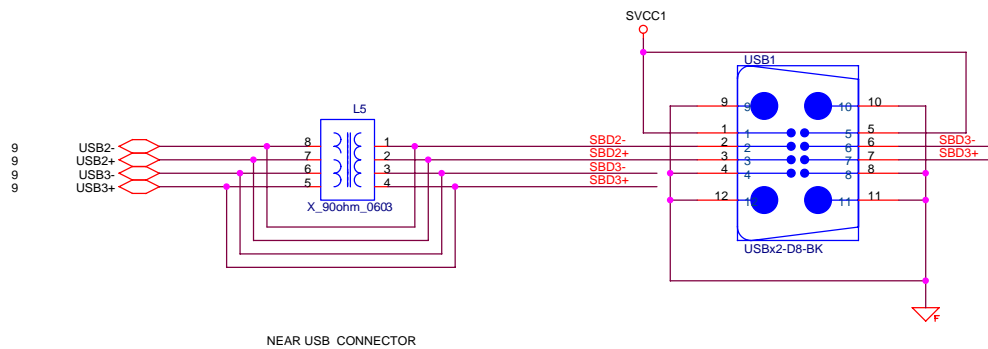
POWER CIRCUIT FOR USB PORT 0,1,2,3



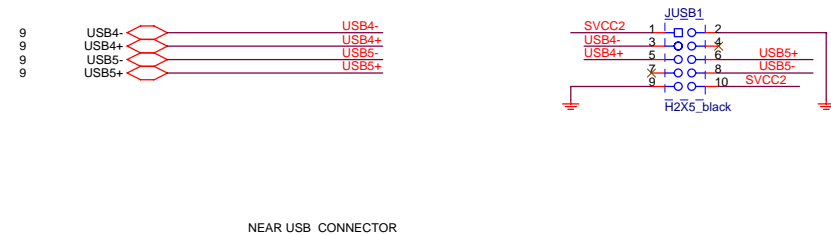
POWER CIRCUIT FOR USB PORT 4,5,6,7



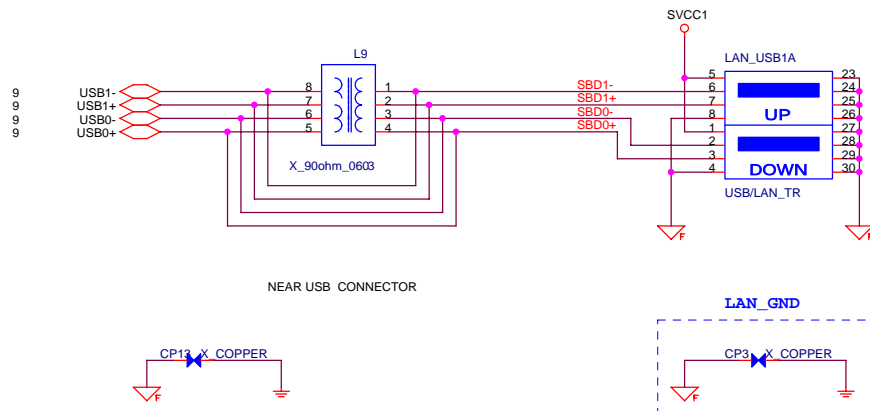
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



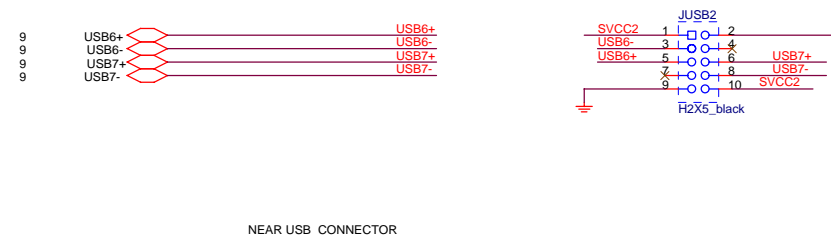
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3

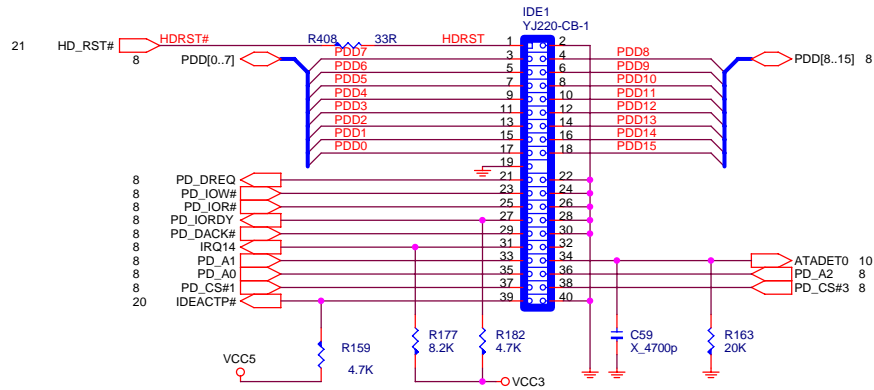


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

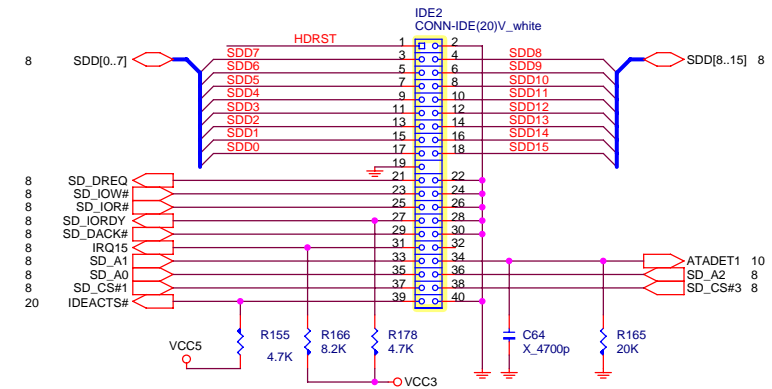


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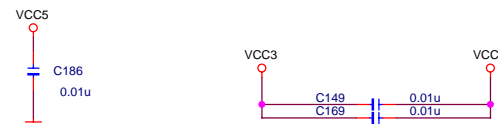
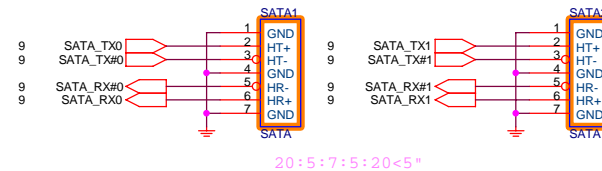
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK

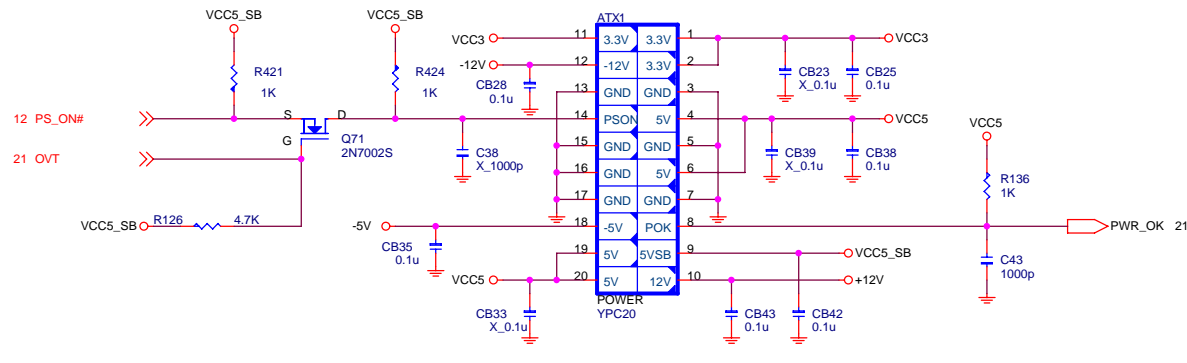


SERIAL ATA CONNECTOR BLOCK

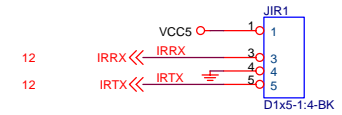


Micro-Star	Title	MS-7038	Rev	1.0A
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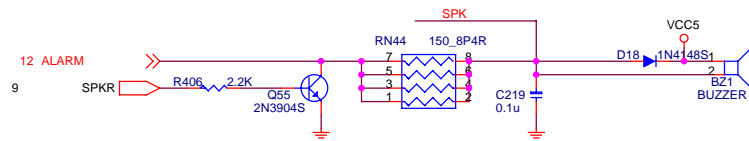
ATX CONNECTOR



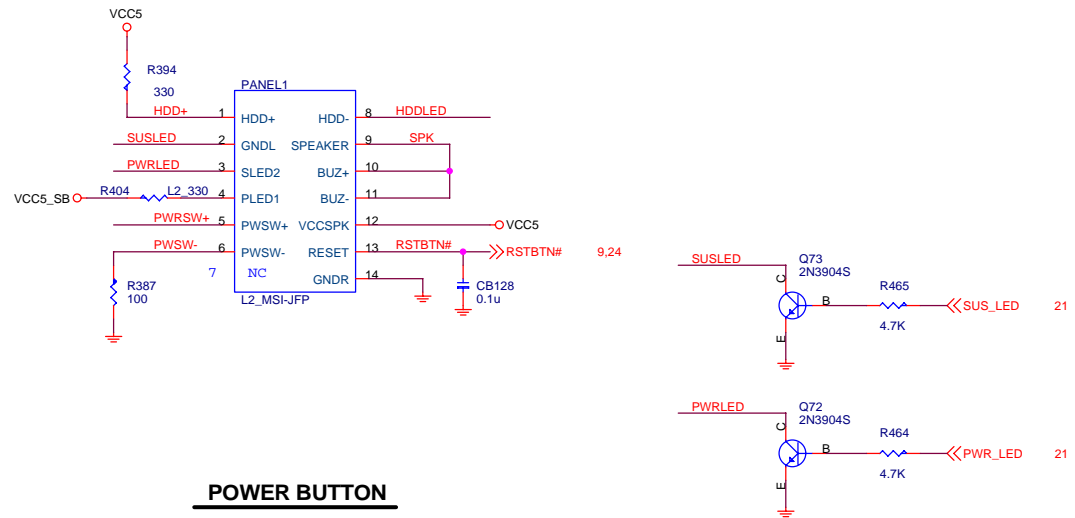
IR CONNECT



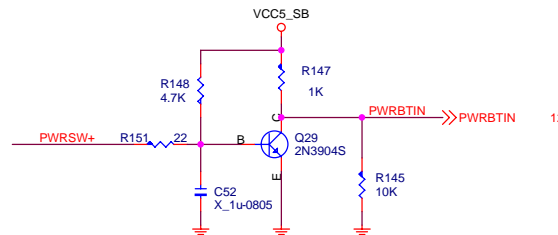
BUZZER



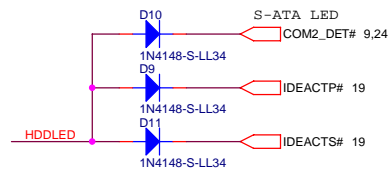
Legend Front Panel



POWER BUTTON



IDE LED



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ACPI Controller

3VSB MODE SELECT
3VSB MODE 3VDLDEC#
SINGLE MOSFET PULL HIGH
DUAL MOSFET PULL LOW

VDIMM LINEAR OR PWM SELECT
VDIMM MODE EXTRAM
LINEAR REGULATOR PULL LOW
PWM REGULATOR PULL HIGH

AGP POWER

$I_o \times R_{ds(on)} = I_{sen}(72\mu A) \times R_{sen}$
 $I_d = 6A, I_d(max) = 24A$
 $R_{ds(on)}/10V = 21m\ ohm \sim 28m\ ohm$
Overcurrent (4.7K ohm) = 12A ~ 16A

Q70 Main source : D03-0731303-A30
Second source : D03-6990A03-F01

5V Dual Power

Rear USB ports

Front USB ports

SWITCH:

D03-40N030B-A36
D03-20N030B-I14
D03-45N030B-P03
Regulator (TO-252)
D03-45N020B-N03
D03-40N030B-A36
D03-603AL1B-C03
D03-6530A0B-F01
Regulator (TO-263)
D03-50N034B-N03
D03-603AL0B-C03
D03-703AL0B-C03

3V Dual Power

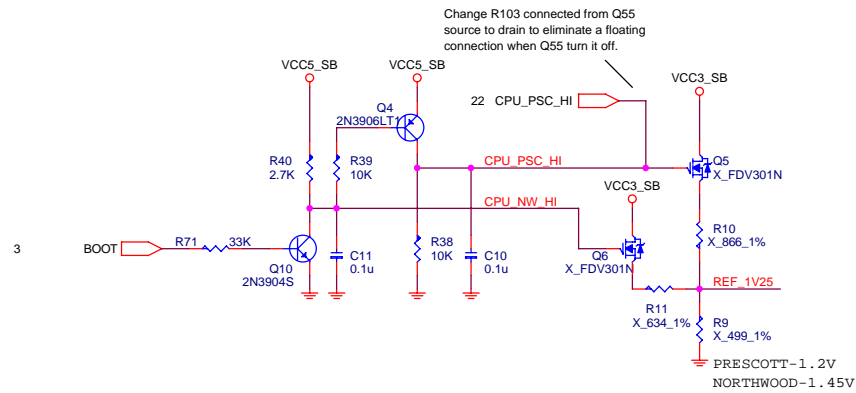
DDR 2.6V Power

DDR VTT Power

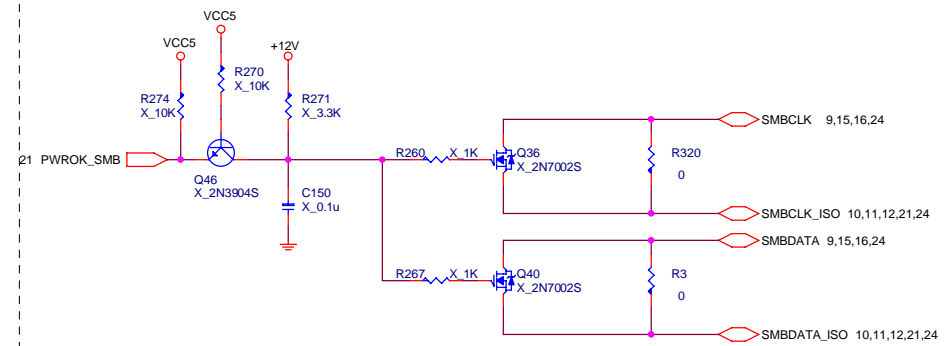
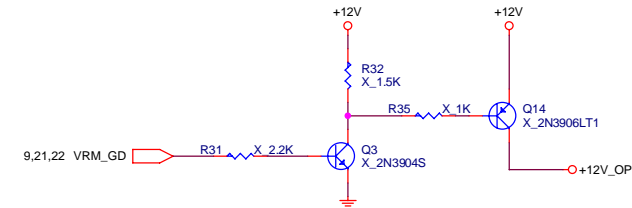
VCC_VID / VID_GOOD

Place MOSFET near CPU

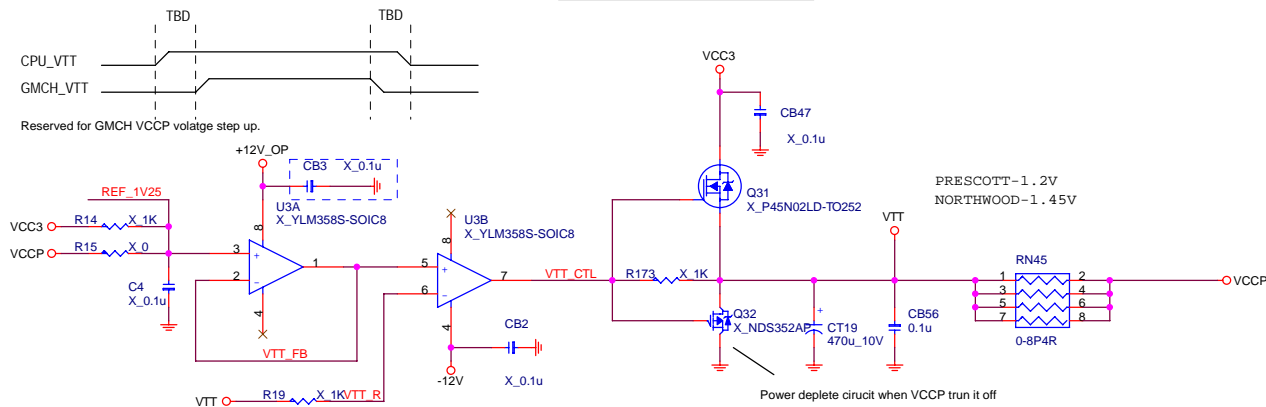
Intel reference GMCH VTT power cirucit



GMCH_VTT ON/OFF CIRCUIT



GMCH VTT Generator



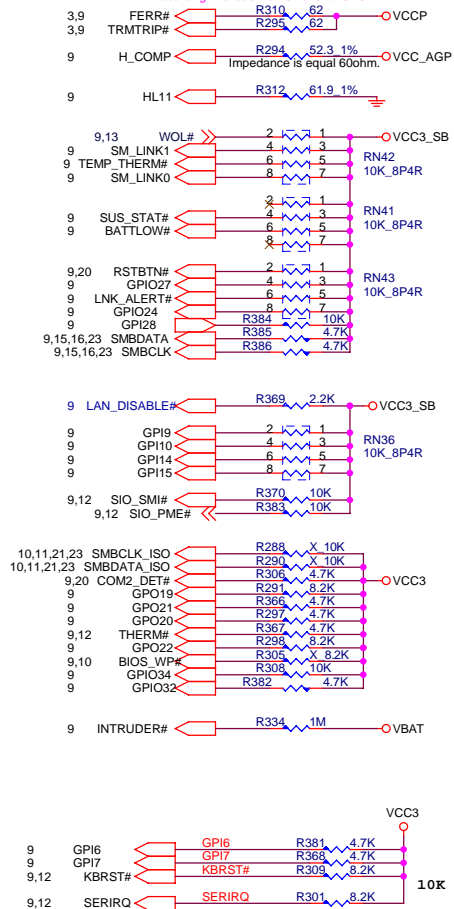
Bootstrip pin are input rather then output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side circuit. And the bootstrip pin power by core voltage so the outside circuit need to adjust the turn off voltage.

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MEM,VCC_DAC & VTT Controller			
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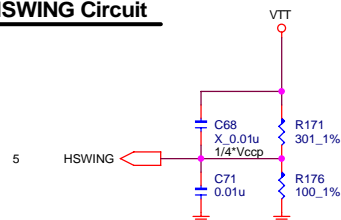
ICH5 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH5

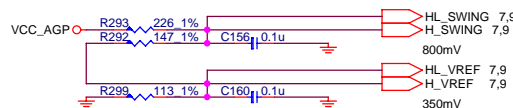
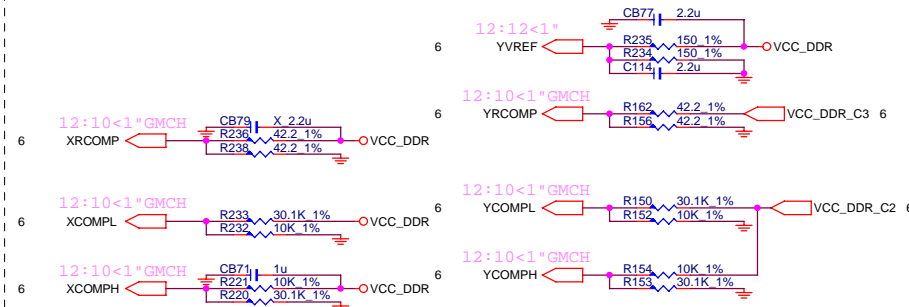
Trace length is less than 3inches to ICH5.



HSWING Circuit

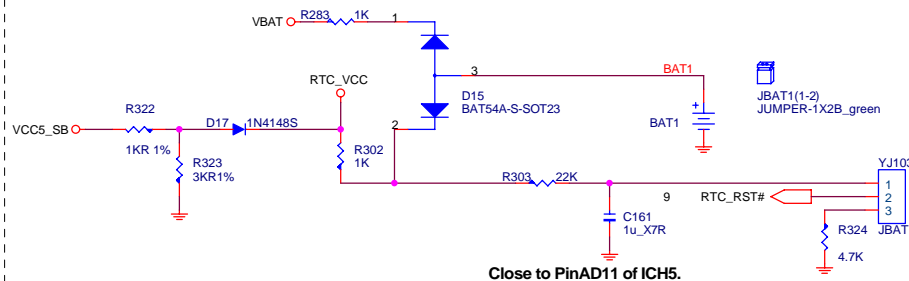


5VREF Sequencing Circuit



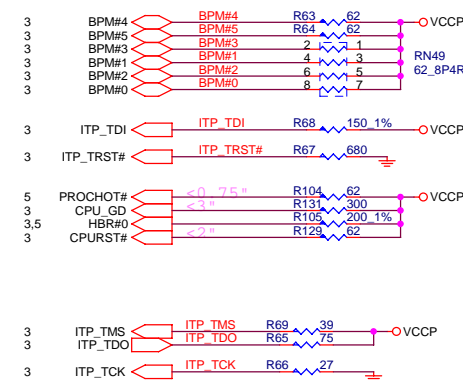
RTC BLOCK

CLR CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



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ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#A	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	WOL#	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	TEMP_THERM#	RESUME
GPIO 12	I	SIO_SMI#	RESUME
GPIO 13	I	GPI13	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	GPO19	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	BIOS_WP#	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	LAN_DISABLE#	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	COM2_DET#	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPU_GD	MAIN

default output
default output
default output
default output
default output
default output

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI slot 1-3, LAN
PCIRST#2	Super I/O,AGP slot
PCIRST_ICH5#	Northbridge , FWH
HDDRST#	Primary, Scondary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#G PIRQ#H PIRQ#E PIRQ#F	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
LAN	PIRQH	PCI_REQ#1 PCI_GNT#1	AD29	LAN_PCLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5

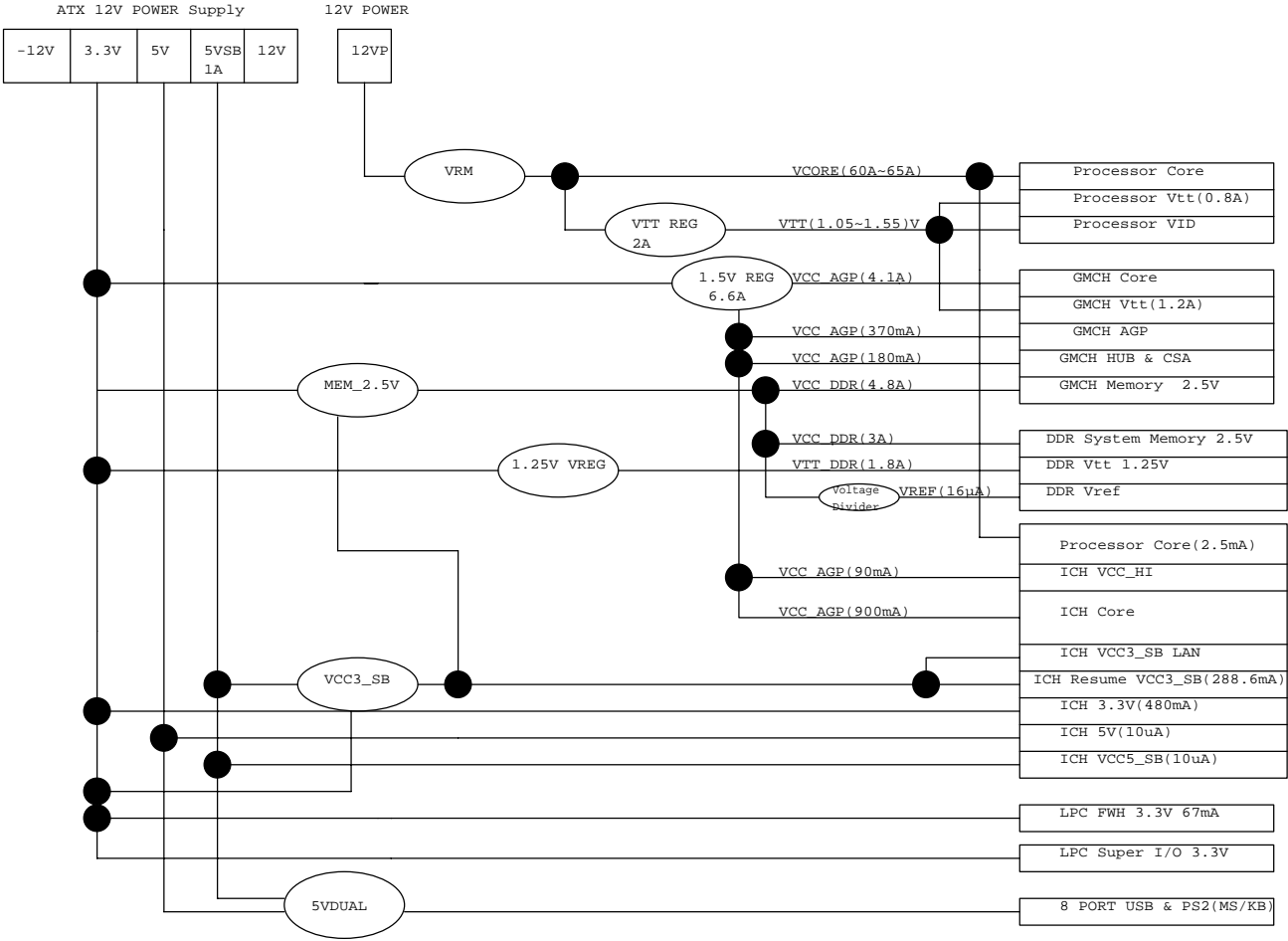
JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
AC	(11-12) W/O FRONT AUDIO (13-14) AUDIO	WITH FRONT AUDIO

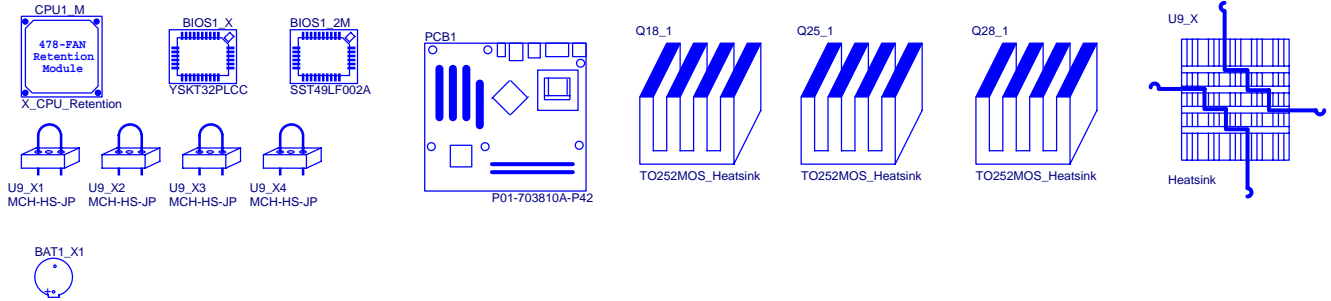
SIO

PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V , High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT / OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-5
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRXX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power.
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

POWER DELIVERY MAP



MANUAL PART



Micro-Star	Title	MS-7038	Rev	1.0A
	Document Number	POWER DELIVERY MAP & MANUAL PART		
	Last Revision Date:	Monday, April 12, 2004	Sheet	26 of 27

Revision History

0B Revision History (Changes from Rev 0A)

Sheet	Description
12	Add TPM function
14	Modify FAN speed control circuit
21	Change ACPI controller from MS-5 to MS-7
21	Change AGP power from NIKO/N2101 to MS-6+
26	Add 3 heatsink on VRM MOS

1.0 Revision History (Changes from Rev 0B)

Sheet	Description
20	Add Q72,Q73,R464,R465 to fix PWR_LED and SUS_LED functions.
12	Connects SIO_PME# with GPI13.